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**Takemura**

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(54) **SEMICONDUCTOR MEMORY DEVICE AND METHOD OF MANUFACTURING SEMICONDUCTOR MEMORY DEVICE**

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CPC ........ ***H01L 27/108*** (2013.01); ***H01L 27/10844*** (2013.01); *H01L 27/1156* (2013.01)

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USPC .......... 365/149, 174, 182, 222; 257/296, 300, 257/E27.084
See application file for complete search history.

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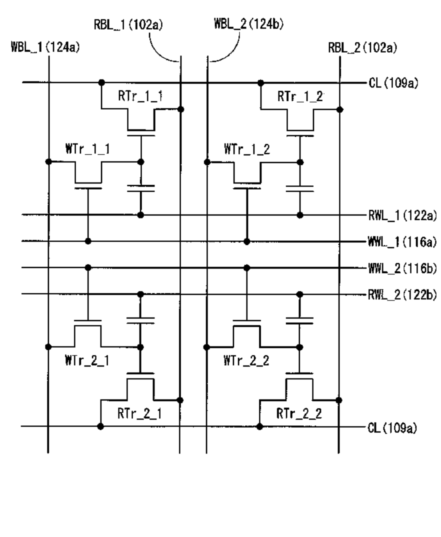
(57) **ABSTRACT**

A highly integrated gain cell-type semiconductor memory is provided. A first insulator, a read bit line, a second insulator, a third insulator, a first semiconductor film, first conductive layers, and the like are formed. A projecting insulator is formed thereover. Then, second semiconductor films and a second gate insulating film are formed to cover the projecting insulator. After that, a conductive film is formed and subjected to anisotropic etching, so that write word lines are formed on side surfaces of the projecting insulator. A third contact plug for connection to a write bit line is formed over a top of the projecting insulator. With such a structure, the area of the memory cell can be $4F^2$ at a minimum.

**10 Claims, 12 Drawing Sheets**



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* cited by examiner

FIG. 1

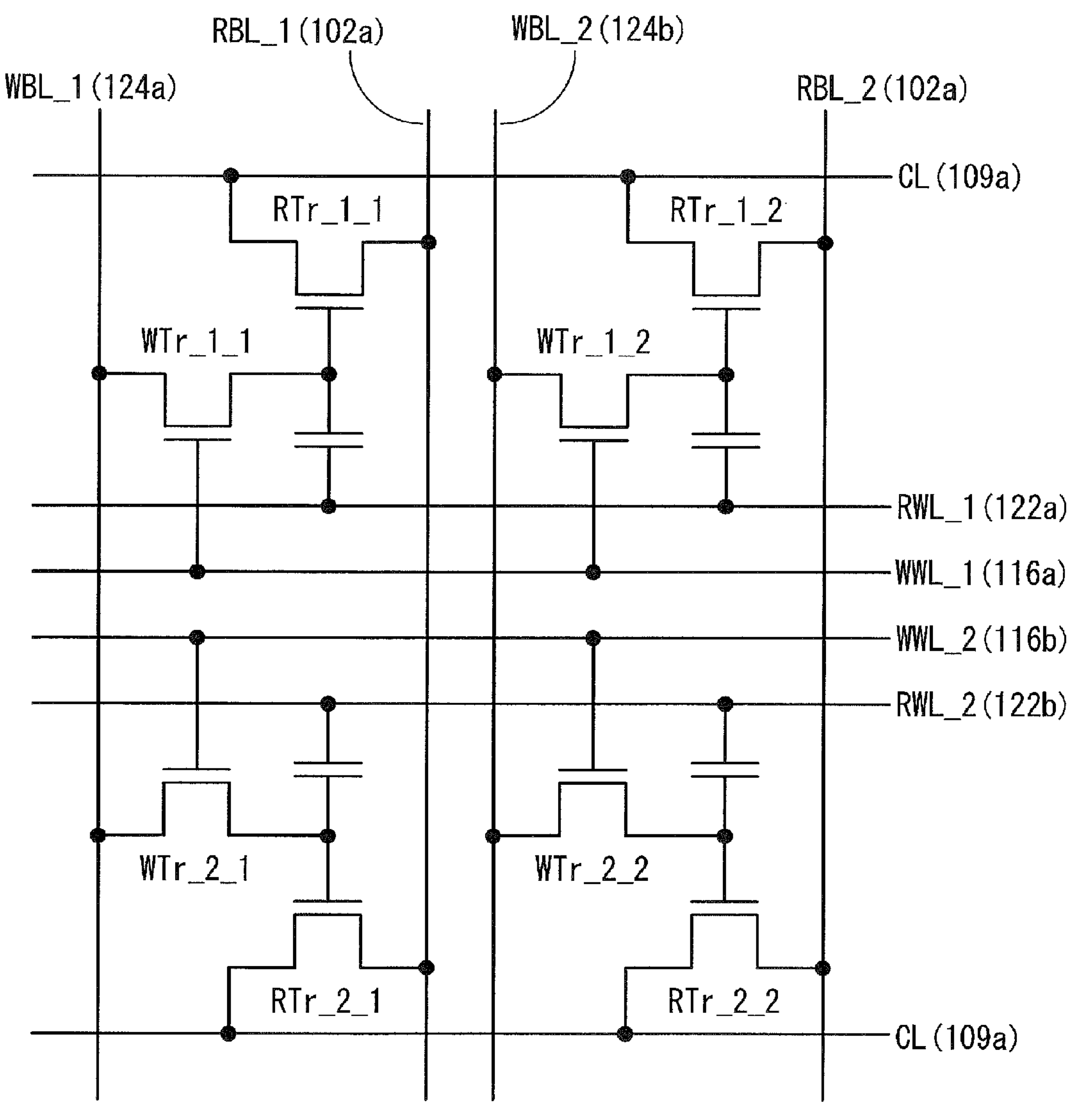

RBL_1 (102a)
WBL_2 (124b)
WBL_1 (124a)
RBL_2 (102a)
CL (109a)
RTr_1_1
RTr_1_2
WTr_1_1
WTr_1_2
RWL_1 (122a)
WWL_1 (116a)
WWL_2 (116b)
RWL_2 (122b)
WTr_2_1
WTr_2_2
RTr_2_1
RTr_2_2
CL (109a)

FIG. 2C

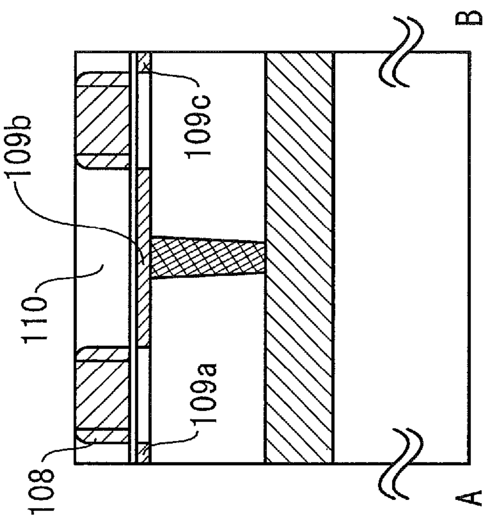



FIG. 2B

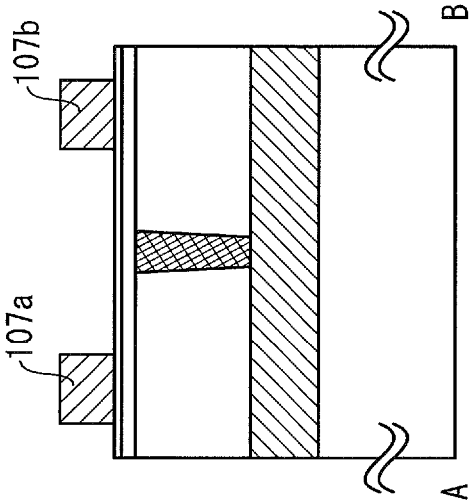



FIG. 2A

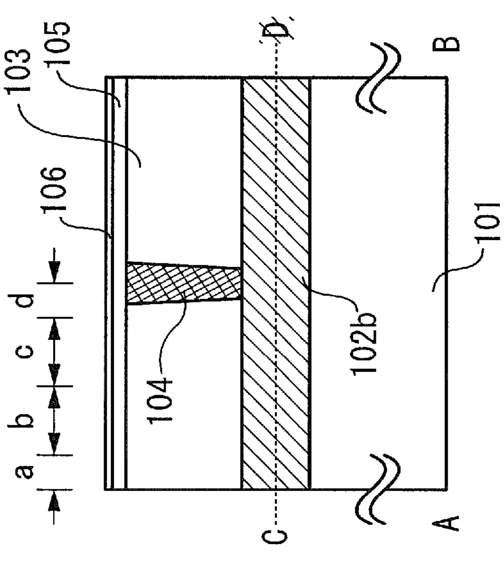


FIG. 3A

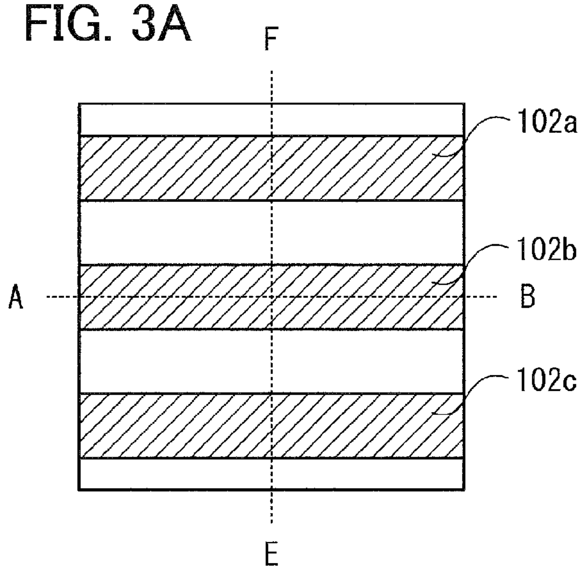



FIG. 3B

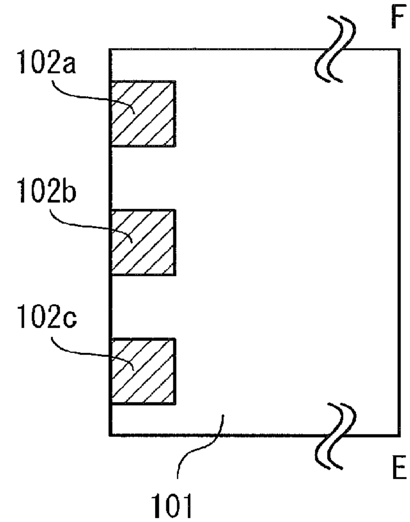



FIG. 3C

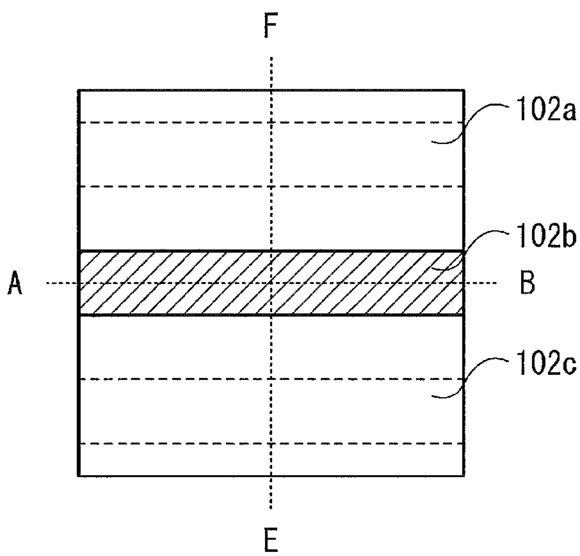



FIG. 3D

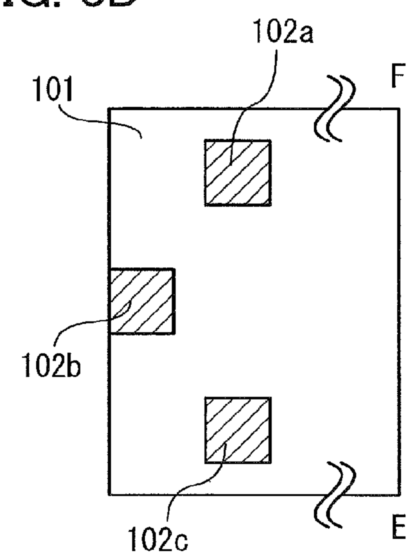


FIG. 4A

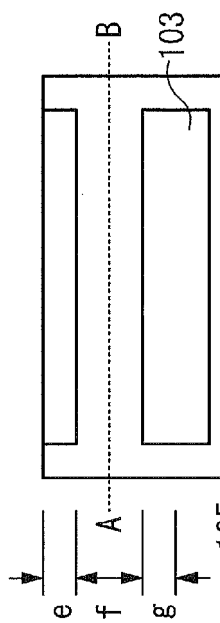



FIG. 4B

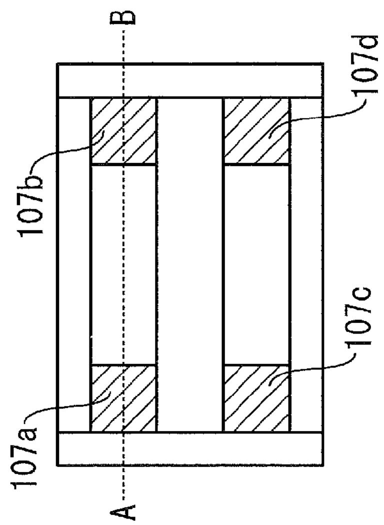



FIG. 4C

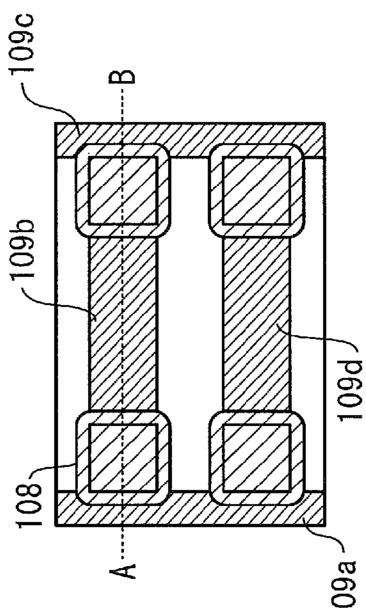


FIG. 5B

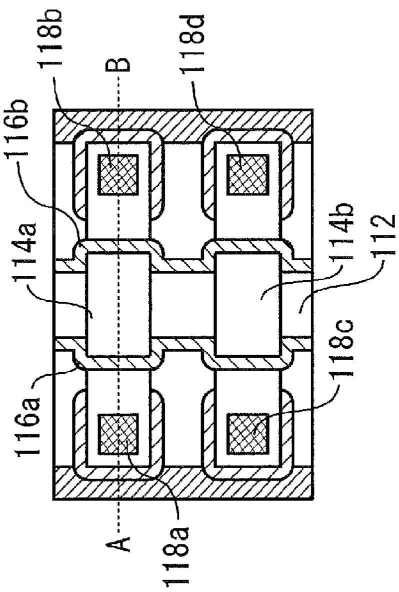



FIG. 5A

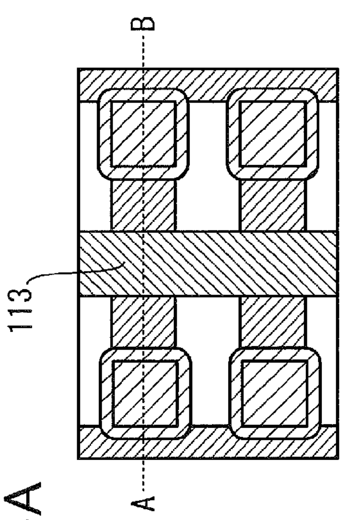



FIG. 5C

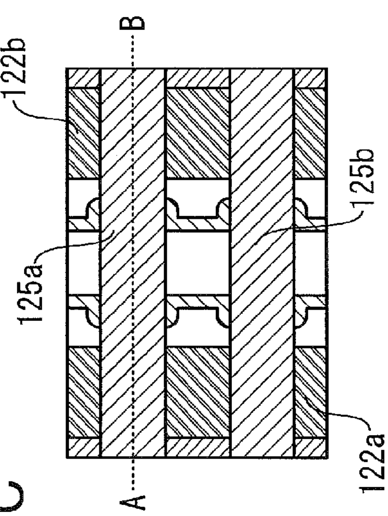


FIG. 6C

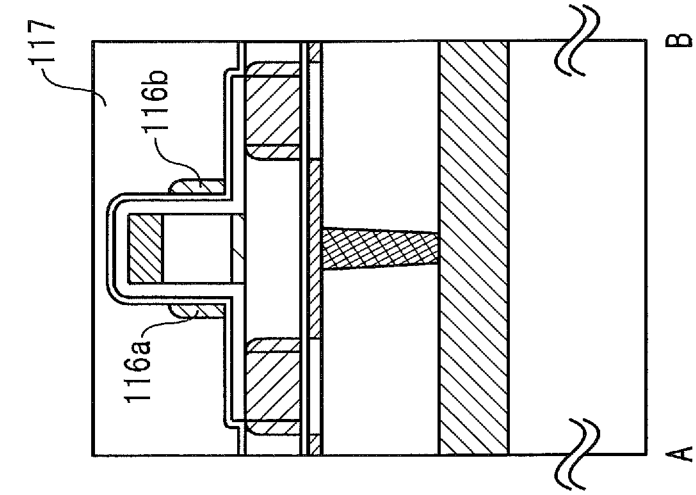



FIG. 6B

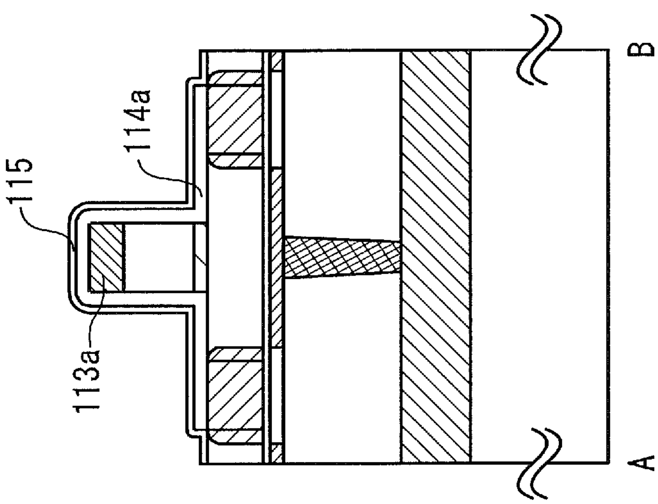



FIG. 6A

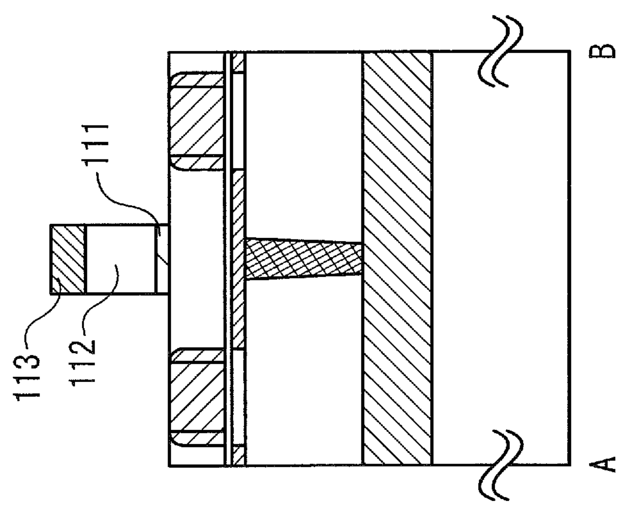


FIG. 7A

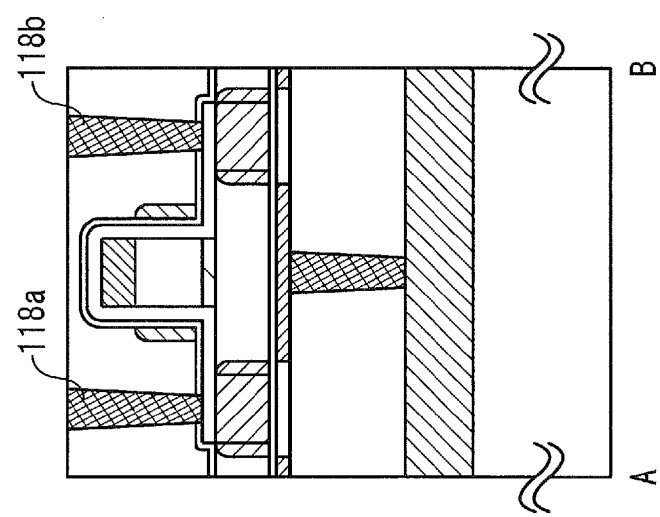



FIG. 7B

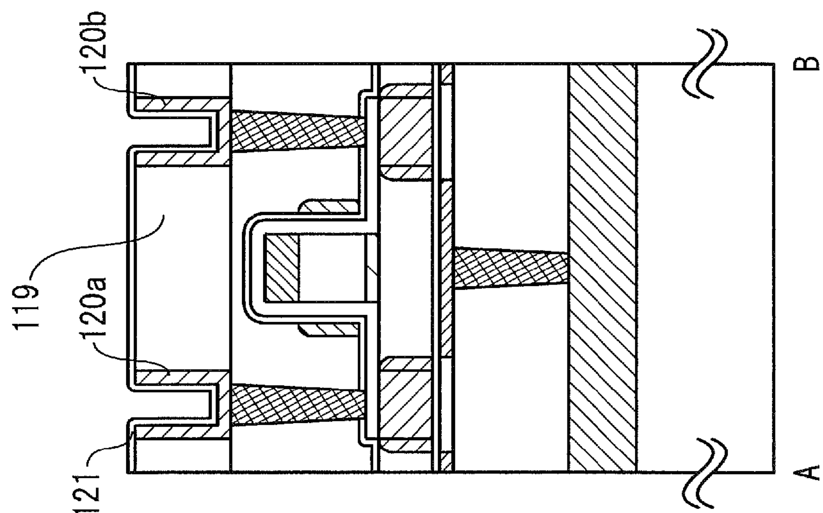



FIG. 7C

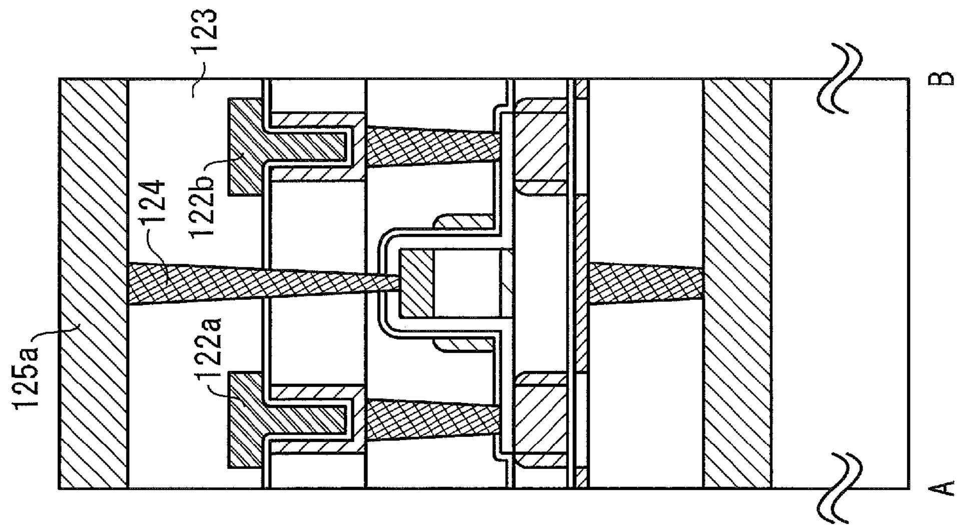


FIG. 8

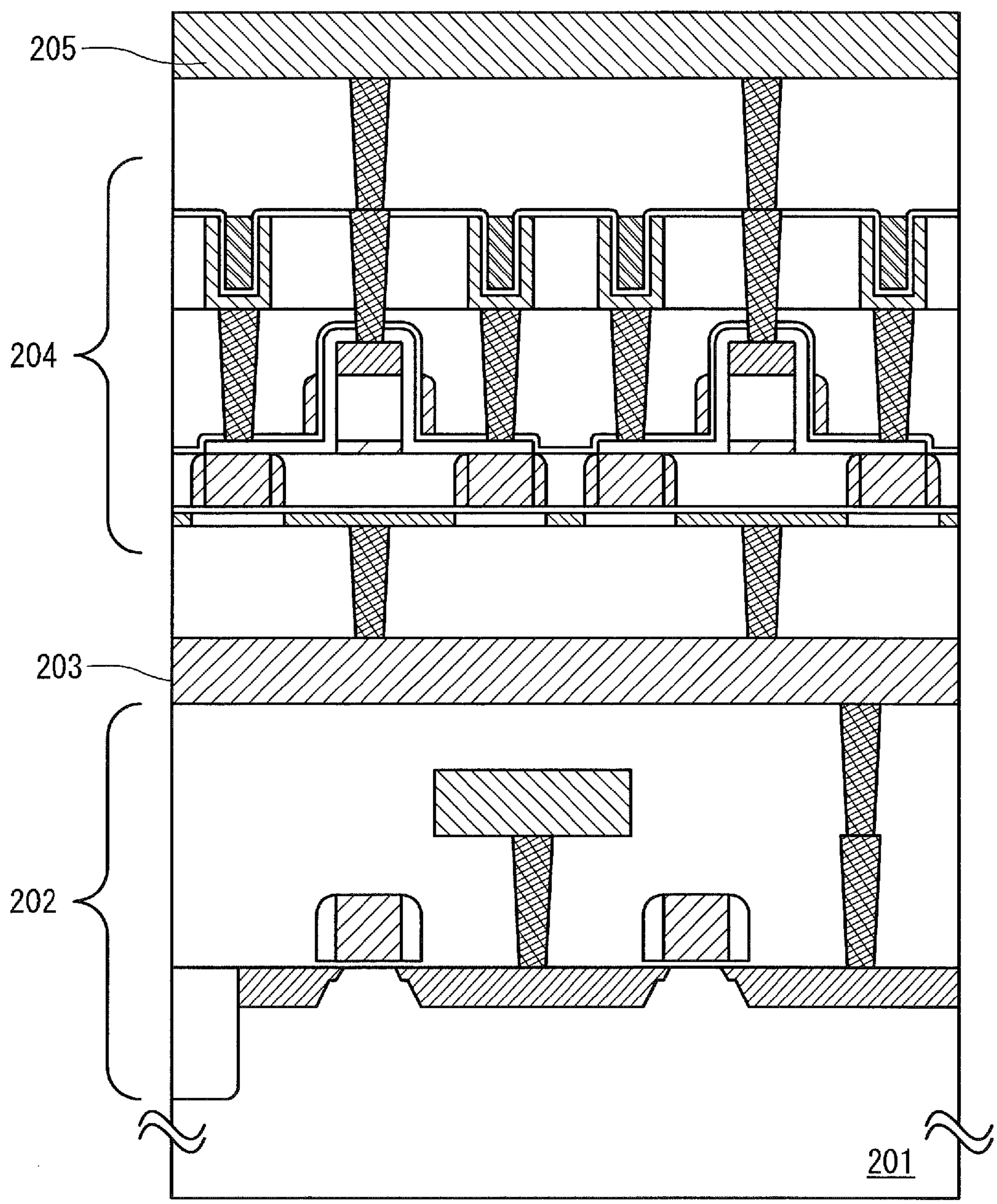


FIG. 9A

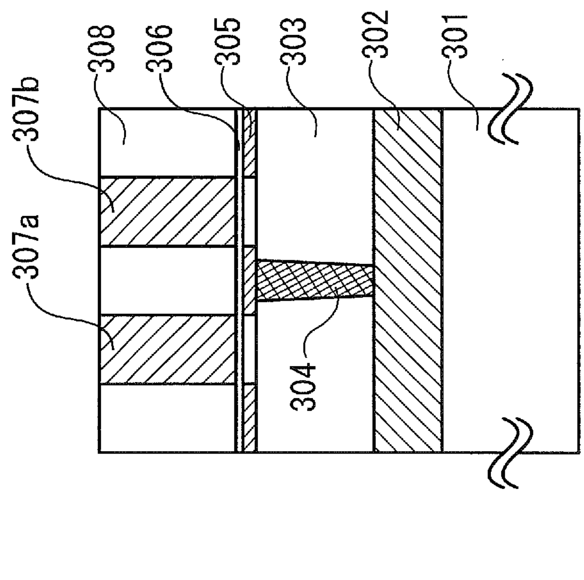



FIG. 9B

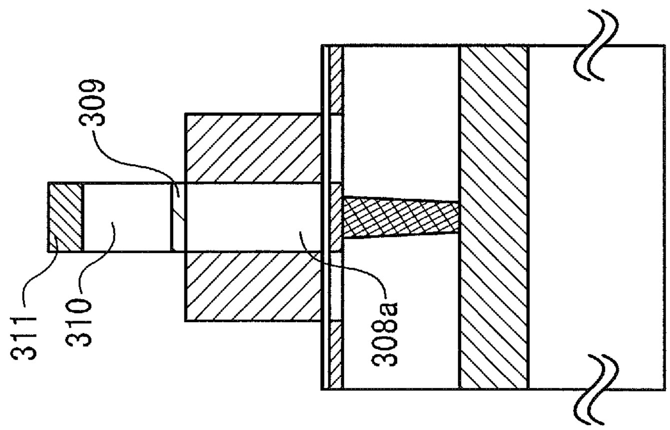



FIG. 9C

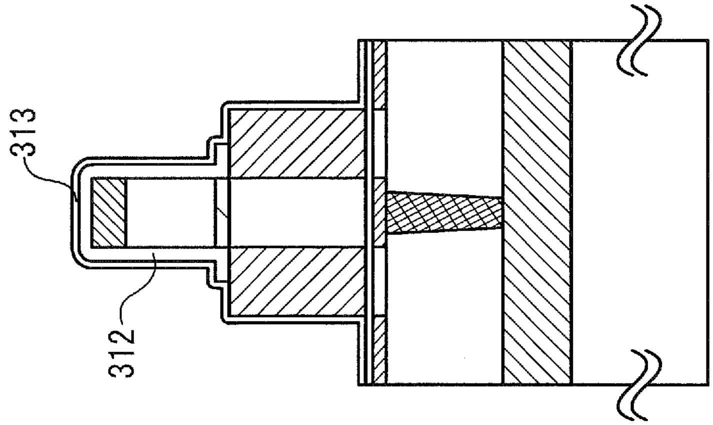


FIG. 10C

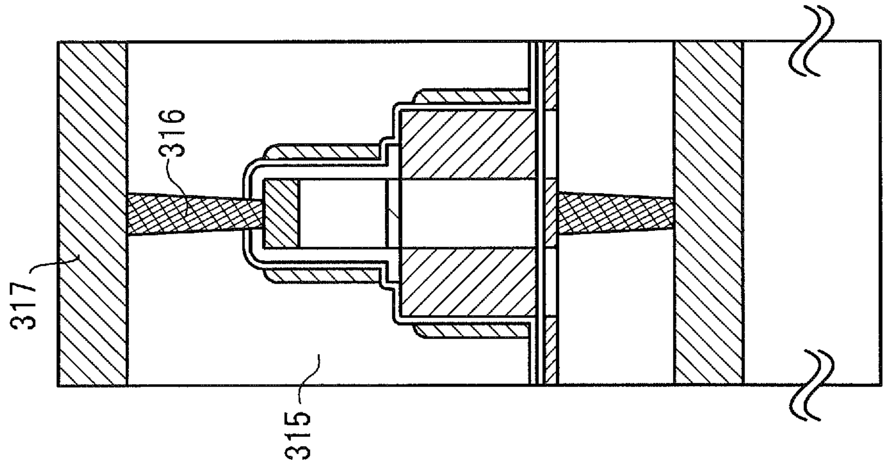



FIG. 10B

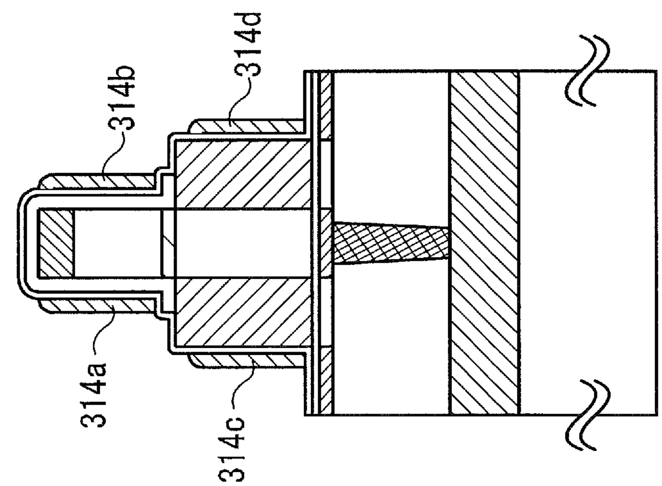



FIG. 10A

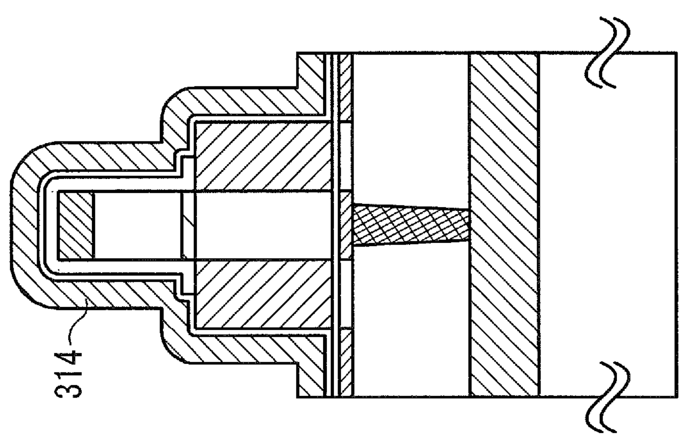


FIG. 11A

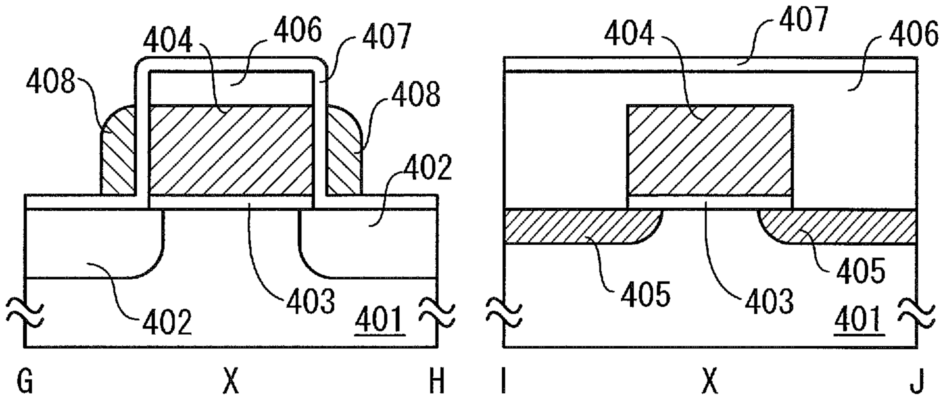



FIG. 11B

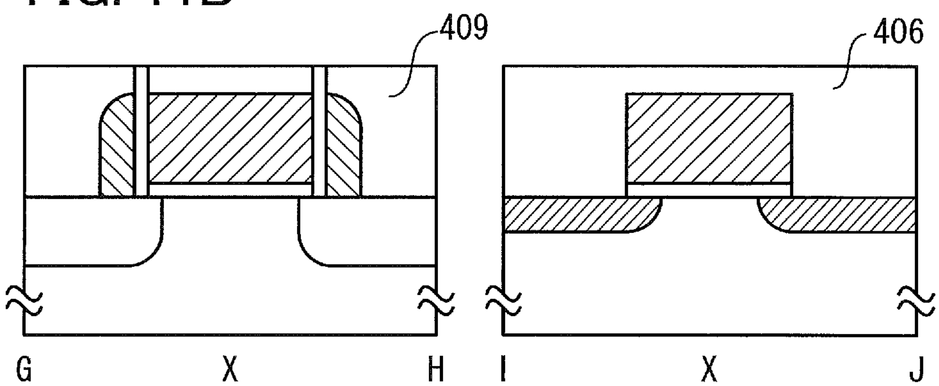



FIG. 11C

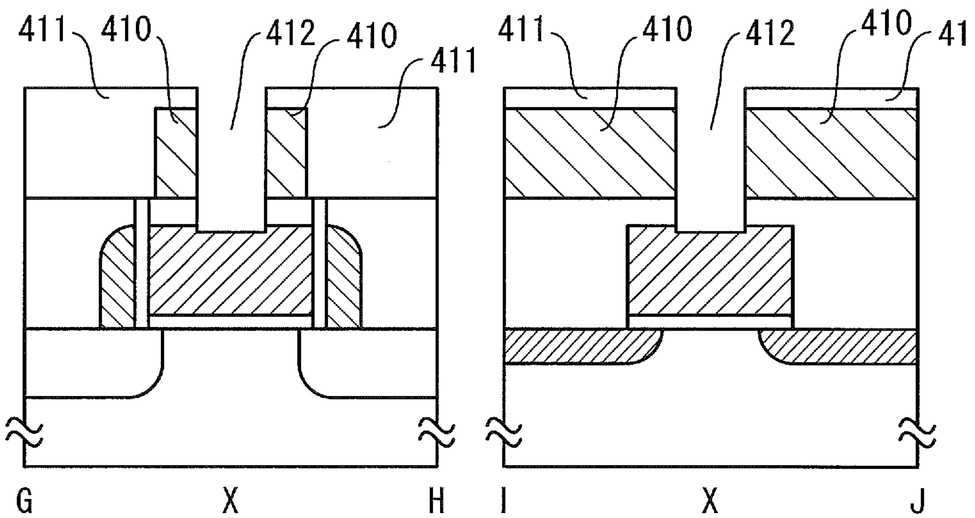


FIG. 12A

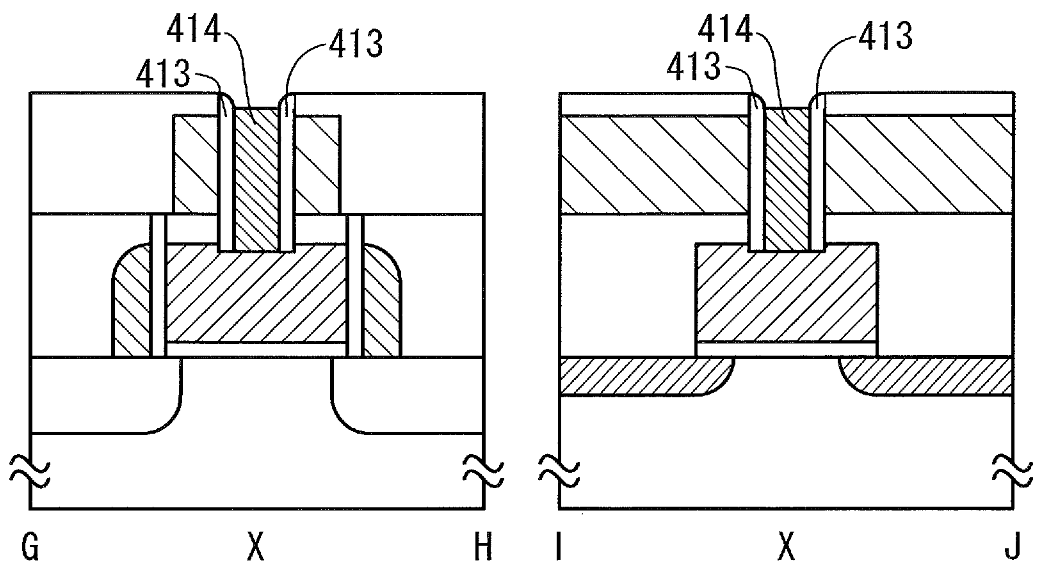
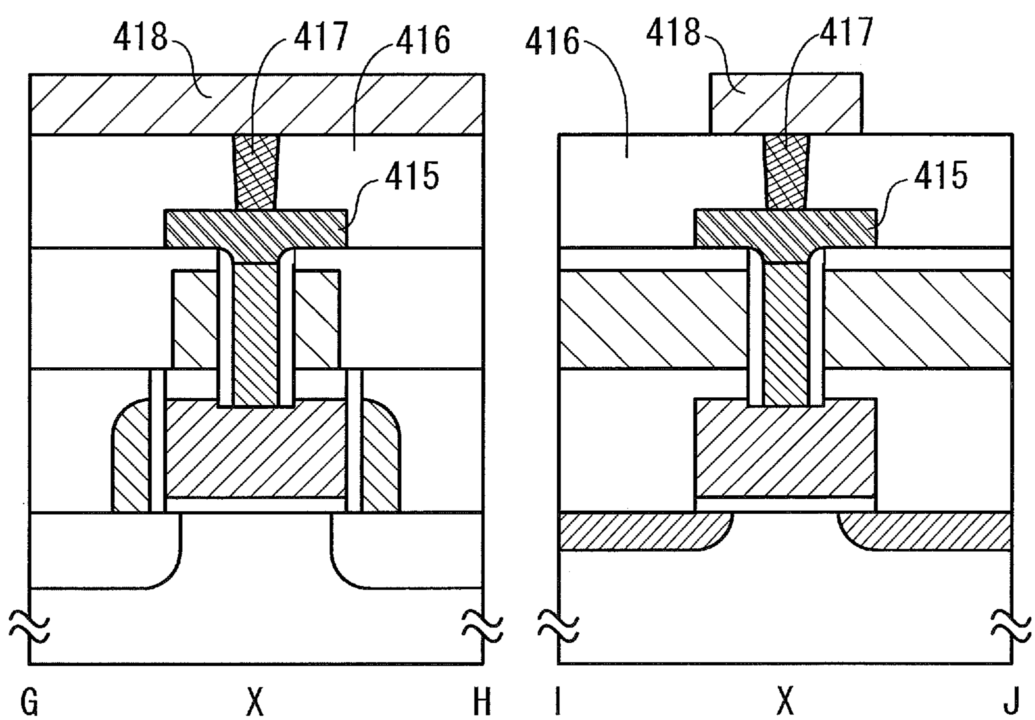



FIG. 12B



# SEMICONDUCTOR MEMORY DEVICE AND METHOD OF MANUFACTURING SEMICONDUCTOR MEMORY DEVICE

## BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor memory device.

2. Description of the Related Art

A dynamic random access memory (1Tr-DRAM) including one capacitor and one transistor (referred to as a cell transistor) has been widely used as a typical semiconductor memory device. However, there is a requirement that the capacitance of the capacitor is not changed even when a circuit is miniaturized, and thus formation of the capacitor is becoming a major hurdle.

Under such a circumstance, a gain cell including two transistors and one capacitor (e.g., see Patent Document 1) has attracted attention as a potential solution for the problem of the conventional 1Tr-DRAM for the following reason. The capacitance of the capacitor in the 1Tr-DRAM is determined by the ratio of the capacitance of the capacitor to the parasitic capacitance of a bit line. In contrast, the capacitance of the capacitor in the gain cell is determined by the ratio of the capacitance of the capacitor to the gate capacitance of a read transistor; therefore, there arises no problem even when the capacitance of the capacitor can be reduced as the size of the transistor is reduced for miniaturization.

A circuit of the gain cell will be briefly described with reference to FIG. **1**. FIG. **1** illustrates four memory cells. Among the memory cells, a memory cell including a write transistor WTr_**1**_**1** will be described. This memory cell includes a read transistor RTr_**1**_**1** and a capacitor in addition to the write transistor WTr_**1**_**1**.

A source of the write transistor WTr_**1**_**1**, a gate of the read transistor RTr_**1**_**1**, and one terminal of the capacitor are connected to each other, thereby forming a memory node. Further, the other terminal of the capacitor is connected to a read word line RWL_**1**, a gate of the write transistor WTr_**1**_**1** is connected to a write word line WWL_**1**, a drain of the write transistor WTr_**1**_**1** is connected to a write bit line WBL_**1**, a drain of the read transistor RTr_**1**_**1** is connected to a read bit line RBL_**1**, and a source of the read transistor RTr_**1**_**1** is connected to a common wiring CL.

Such memory cells are arranged in matrix and connected by write word lines WWL, write bit lines WBL, read word lines RWL, read bit lines RBL, common wirings CL, and the like.

## REFERENCE

### Patent Document


[Patent Document 1] U.S. Pat. No. 7,468,901
[Patent Document 2] U.S. Pat. No. 7,772,053
[Patent Document 3] United States Patent Application Publication No. 2011/0205774
[Patent Document 4] U.S. Pat. No. 5,302,843


## SUMMARY OF THE INVENTION

However, enough consideration of an increase in the integration degree of a gain cell has not been made. Since the gain cell includes two transistors and thus needs a large area for one memory cell when the transistors are arranged in one



plane, it is difficult to achieve a cell area as small as $6F^2$ (F is a feature size) unlike a 1Tr-DRAM.

In addition, a write transistor in the gain cell needs to have sufficiently high off-state resistance. For example, in the case where the capacitance of a capacitor is 1/1000 of that of a capacitor in a 1Tr-DRAM, charges accumulated in the capacitor in the gain cell is lost 1000 times as quickly as that in the 1Tr-DRAM when the off-state resistance of the write transistor is assumed to be equal to the off-state resistance of a cell transistor in the 1Tr-DRAM. Therefore, refresh is needed **1000** times as frequently as that for the 1Tr-DRAM.

Further, when the circuit is miniaturized, the subthreshold characteristics of the write transistor deteriorate because of a short-channel effect and the off-state resistance thereof tends to decrease; no effective solutions for this problem have been proposed.

The present invention has been made in view of the above problems and its object is, for example, to provide a semiconductor memory device whose area can be reduced as much as possible, a configuration of a circuit of the semiconductor memory device, and/or a method of manufacturing the semiconductor memory device. Another object is to provide a semiconductor memory device in which the parasitic capacitance of a bit line can be reduced, a configuration of a circuit of the semiconductor memory device, and/or a method of manufacturing the semiconductor memory device. Further, another object of the present invention is to provide a highly reliable semiconductor device with excellent characteristics and/or a method of manufacturing the semiconductor device.

One mode of the present invention is a semiconductor memory device including a read bit line formed over a substrate, a first semiconductor film formed over the read bit line, a projecting insulator formed over the first semiconductor film, two write word lines that are formed on side surfaces of the projecting insulator and face each other with the insulator interposed therebetween, a second semiconductor film interposed between the write word lines and the side surfaces of the projecting insulator, an electrode provided over a top of the projecting insulator, and a write bit line that is provided over the projecting insulator and is electrically connected to the electrode.

In this specification, a read bit line may be considered as a wiring connected to a sense amplifier or another circuit, or as a wiring whose potential is amplified by a sense amplifier. A write word line may be considered as a wiring connected to a gate of a write transistor.

Here, the read bit line is preferably electrically connected to the first semiconductor film. Electrical connection means that components are connected with one or more materials having practically sufficiently low resistance interposed therebetween. Further, the height of the projecting insulator is preferably greater than or equal to 1 time and less than or equal to 20 times, further preferably greater than or equal to 2 times and less than or equal to 20 times the distance between the projecting insulator and another projecting insulator. The height of the write word line is preferably greater than or equal to 30% and less than or equal to 90%, further preferably greater than or equal to 40% and less than or equal to 80% of the height of the projecting insulator.

Another mode of the present invention is a method of manufacturing a semiconductor memory device, including the steps of forming a read bit line over a first insulator, forming a second insulator over the read bit line, forming a first contact hole in the second insulator, forming a first semiconductor film over the second insulator, forming a third insulator over the first semiconductor film, forming a projecting insulator by etching the third insulator, providing an island-shaped or stripe-shaped second semiconductor film in a region including a side surface of the projecting insulator, forming a conductive film, forming a write word line on the side surface of the projecting insulator by anisotropically etching the conductive film, forming a fourth insulator, forming a second contact hole reaching a top of the projecting insulator by etching the fourth insulator, and forming a write bit line over the fourth insulator.

In the step of etching the third insulator and the step of forming the second contact hole reaching the top of the projecting insulator, another film serving as an etching stopper may be used to control the etching.

In any of the above modes, a driver circuit such as a sense amplifier or a decoder may be provided below the read bit line. The read bit line and another read bit line adjacent thereto may be different from each other in height or depth.

In any of the above modes, a semiconductor region is preferably formed of a semiconductor with a mobility higher than or equal to 5 $cm^2/Vs$. For example, polycrystalline silicon, polycrystalline germanium, polycrystalline silicon germanium, indium oxide, an oxide obtained by adding one or more kinds of metal elements to indium oxide, gallium nitride, a compound obtained by adding oxygen to gallium nitride, gallium arsenide, indium arsenide, or zinc sulfide may be used.

Although a structure in which a gate of a transistor is provided on a side surface of a projection and/or a depression formed in a semiconductor substrate with the use of anisotropic etching is known (e.g., Patent Document 4), a preferable mode in the case of increasing the integration degree of a semiconductor memory using this structure has not been considered. Moreover, enough consideration has not been made for a preferable mode for suppression of a short-channel effect of such a transistor or a preferable application mode to a gain cell. These modes are sufficiently considered in the present invention.

By employing at least one of technical ideas disclosed in the above modes and embodiments below, the channel length of the write transistor is determined in accordance with the height of the projecting insulator. Therefore, when the height of the projecting insulator is 300 nm and the height of the write word line is 300 nm for example, the channel length of the write transistor can be 300 nm, while the channel width can be set to a feature size (e.g., 30 nm).

The on-state resistance of the write transistor is 10 times that of a planar transistor whose channel length and channel width are each 30 nm. Meanwhile, the off-state resistance of the write transistor can be, for example, greater than or equal to 1000 times, preferably greater than or equal to 10000 times that of the planar transistor as a result of suppression of a short-channel effect. Such a cell is compared with a cell of a 1Tr-DRAM. Even if the field effect mobility of the write transistor in the above mode is 1/10 of the mobility of single crystal silicon used in the 1Tr-DRAM, the cell of the above mode is advantageous over the cell of the 1Tr-DRAM according to the discussion below. In this case, the write transistor has a mobility that is 1/10 of that of a transistor in the 1Tr-DRAM and a channel length that is 10 times that of a transistor in the 1Tr-DRAM; therefore, the on-state resistance of the write transistor is 100 times that of the transistor in the 1Tr-DRAM.

Meanwhile, the capacitance of the capacitor in the 1Tr-DRAM is 30 fF, whereas the capacitance of the capacitor in the gain cell may be, for example, greater than or equal to one time the gate capacitance of a read transistor. Since the gate capacitance of the planar transistor whose channel length and channel width are each 30 nm is several ten attofarads (aF), the capacitance of the capacitor in the gain cell is set to 300 aF (=0.3fF) here. That is, the capacitance (30 fF) of the capacitor in the 1Tr-DRAM is 100 times the capacitance of the capacitor in the gain cell.

On the other hand, the on-state resistance of a cell transistor in the 1Tr-DRAM is 1/100 of the on-state resistance of the write transistor in the gain cell. However, time taken for writing is determined by the product of the on-state resistance and the capacitance of a capacitor; therefore, time taken for writing data into the cell of the 1Tr-DRAM is equal to that taken for the gain cell.

Note that insufficient off-state resistance requires an increase in refresh frequency and makes the gain cell impractical. The off-state resistance of the write transistor needs to be greater than or equal to 100 times the off-state resistance of the cell transistor in the 1Tr-DRAM in order to take the above advantage, otherwise the refresh frequency is higher than that of the 1Tr-DRAM.

In this respect, since owing to the mobility and channel length of the write transistor, the off-state resistance of the write transistor is 100 times the off-state resistance of the cell transistor in the 1Tr-DRAM, the refresh frequency of the gain cell can be equal to that of the 1Tr-DRAM. Moreover, the large channel length of the write transistor can suppress a short-channel effect, and thus the off-state resistance thereof is further increased. As a result, the refresh frequency becomes lower than that of the 1Tr-DRAM, and power consumption in a standby mode can be reduced.

It is obvious from the above discussion that, in a gain cell, an increase in the off-state resistance of a transistor is more important than the mobility thereof, which is certainly an important element though. In other words, the above discussion indicates that, when the ratio between on-state resistance and off-state resistance (on/off ratio=off-state resistance/on-state resistance) is a value with 10 digits or more, preferably a value with 20 digits or more, the transistor can be used as a write transistor in the gain cell whatever semiconductor material is used therein.

For example, use of a semiconductor material with which the on/off ratio becomes a value with 20 digits enables the refresh frequency to be significantly reduced; for example, it is enough to perform refresh less than or equal to once a year.

Further, more importance is placed on an increase in integration degree. The off-state resistance can be increased by increasing the channel length in general, which is a measure against miniaturization. In this respect, by employing any one of the above modes and the embodiments below, the area of the memory cell can be less than or equal to $6F^2$, for example, $5F^2$.

In any one of the above modes and the embodiments below, a projecting insulator having a high aspect ratio needs to be formed. Note that the projecting insulator has a feature which is completely different from that of a capacitor having a high aspect ratio in the 1Tr-DRAM.

A stacked capacitor or a trench capacitor is used in the 1Tr-DRAM. In the 1Tr-DRAM, the capacitor is required to have constant capacitance even when the element size is reduced. For example, when the feature size is reduced to 1/10, the height or depth of the capacitor needs to be increased by 100-fold. In contrast, the height of the projecting insulator according to any one of the above modes and the embodiments below does not need to depend on the feature size.

For example, the feature size can be reduced to 1/10 without changing the height of the projecting insulator. In that case, the channel width of the write transistor provided on the side surface of the projecting insulator is reduced to 1/10. That is, the off-state resistance of the write transistor is increased by 10-fold. Meanwhile, although the gate capacitance of the read transistor is reduced to 1/100, the capacitance of the capacitor is not necessarily proportional to the gate capacitance of the read transistor and thus can be kept at 1/10 depending on the degree of miniaturization. In this case, the refresh frequency is not changed from that before miniaturization.

The height of the write word line is set to 300 nm in the above description; in an actual case, however, in consideration of process margin or the like, the height of the write word line is preferably set to be greater than or equal to 30% and less than or equal to 90%, further preferably greater than or equal to 40% and less than or equal to 80% of the height of the projecting insulator. For example, when the height of the write word line is 50% of the height of the projecting insulator, the channel length is approximately 150 nm.

In the above example, the channel length is 10 times the channel width. In such a transistor having a large channel length, variation in threshold voltage can be small in the case of using particularly a polycrystalline semiconductor material.

In the above structure, the read bit line is provided below the first semiconductor film and a component which can be an obstacle is not particularly provided in that portion, so that the depth at which the read bit line is arranged can be set as appropriate. Needless to say, the read bit line can be formed apart from the transistor (that is, in a deep position) to further reduce the parasitic capacitance. Further, the depth of one read bit line is set to be different from the depth of another read bit line adjacent thereto, whereby the parasitic capacitance generated between the adjacent read bit lines can also be reduced.

Furthermore, since the read bit line is positioned apart from the capacitor, the write word line, and the like, the parasitic capacitance between the read bit line and such components can also be reduced and signal delay can be suppressed.

By providing a circuit for driving the read bit line below the read bit line, the chip area can be reduced. In general, a driver circuit occupies 20% to 50% of a surface of a DRAM chip, which also applies to the gain cell. When the driver circuit and a memory cell array overlap with each other, the chip area can be reduced, or a larger number of memory cells can be formed than in the case of a conventional DRAM having the same chip area. The driver circuit is preferably formed using a single crystal semiconductor.

## BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

FIG. **1** illustrates an example of a circuit of a semiconductor memory device according to Embodiment 1;

FIGS. **2**A to **2**C illustrate an example of a manufacturing process of a semiconductor memory device according to Embodiment 1;

FIGS. **3**A to **3**D illustrate an example of a manufacturing process of a semiconductor memory device according to Embodiment 1;

FIGS. **4**A to **4**C illustrate an example of a manufacturing process of a semiconductor memory device according to Embodiment 1;

FIGS. **5**A to **5**C illustrate an example of a manufacturing process of a semiconductor memory device according to Embodiment 1;

FIGS. **6**A to **6**C illustrate an example of a manufacturing process of a semiconductor memory device according to Embodiment 1;

FIGS. **7**A to **7**C illustrate an example of a manufacturing process of a semiconductor memory device according to Embodiment 1;

FIG. **8** illustrates an example of a structure of a semiconductor memory device according to Embodiment 2;

FIGS. **9**A to **9**C illustrate an example of a manufacturing process of a semiconductor memory device according to Embodiment 3;

FIGS. **10**A to **10**C illustrate an example of a manufacturing process of a semiconductor memory device according to Embodiment 3;

FIGS. **11**A to **11**C illustrate an example of a manufacturing process of a semiconductor memory device according to Embodiment 4; and

FIGS. **12**A and **12**B illustrate an example of a manufacturing process of a semiconductor memory device according to Embodiment 4.

## DETAILED DESCRIPTION OF THE INVENTION

Hereinafter, embodiments will be described with reference to drawings. Note that the embodiments can be implemented with various modes. It will be readily appreciated by those skilled in the art that modes and details can be changed in various ways without departing from the spirit and scope of the present invention. Thus, the present invention should not be construed as being limited to the description of the following embodiments.

In this specification, ordinal numbers such as “first” and “second” are used to avoid confusion among components and do not necessarily mean the order. For example, another insulator may be provided below a first insulator, or another contact plug may be provided between a first contact plug and a second contact plug.

In this specification, “source” and “drain” are terms referring to terminals of a transistor for distinguishing them from each other; a terminal referred to as a source in this specification may be regarded as a drain.

(Embodiment 1)

A manufacturing process of a memory cell according this embodiment will be described with reference to FIGS. **2**A to **2**C, FIGS. **3**A to **3**D, FIGS. **4**A to **4**C, FIGS. **5**A to **5**C, FIGS. **6**A to **6**C, and FIGS. **7**A to **7**C. FIGS. **2**A to **2**C, FIGS. **6**A to **6**C, and FIGS. **7**A to **7**C each illustrate a cross section parallel to a bit line in the memory cell according to this embodiment. FIGS. **4**A to **4**C and FIGS. **5**A to **5**C are schematic views each illustrating a manufacturing step in the case where the memory cell according to this embodiment is seen from the above. Note that an insulating film or the like is not illustrated in FIGS. **4**A to **4**C and FIGS. **5**A to **5**C. Cross sections along dotted line A-B in FIGS. **4**A to **4**C and FIGS. **5**A to **5**C correspond to FIGS. **2**A to **2**C, FIGS. **6**A to **6**C, and FIGS. **7**A to **7**C.

In this embodiment, with a few exceptions, just the outline is described. Known techniques for forming a semiconductor integrated circuit or the like may be referred to for the details. FIGS. **2**A to **2**C, FIGS. **6**A to **6**C, and FIGS. **7**A to **7**C will be described below in this order. Other drawings are also used as needed.

<FIG **2**A>

Read bit lines **102***a* to **102***c* (note that the read bit lines **102***a* and **102***c* are illustrated only in FIGS. **3**A to **3**D) are formed over a first insulator **101**. There are some methods for arrangement of the read bit line **102***b* and the read bit lines **102***a* and **102***c* adjacent to the read bit line **102***b*. A first method is a method in which, as illustrated in FIGS. **3**A and

3B, the read bit lines **102**_a_ and **102**_c_ adjacent to the read bit line **102**_b_ are formed at the same depth or in the same layer as the read bit line **102**_b_.

FIG. **3**A is a schematic view of a cross section obtained by cutting a plane in which the read bit lines **102**_a_ to **102**_c_ are formed along a plane including dotted line C-D in FIG. **2**A. FIG. **3**B illustrates a cross section along dotted line E-F in FIG. **3**A. Note that FIG. **2**A illustrates a cross section along dotted line A-B in FIGS. **3**A and **3**C.

As illustrated in FIG. **3**B, the read bit line **102**_b_ is formed at the same depth or in the same layer as the read bit lines **102**_a_ and **102**_c_ adjacent to the read bit line **102**_b_. This method has a feature of fewer manufacturing steps.

Another method is a method in which, as illustrated in FIGS. **3**C and **3**D, the read bit lines **102**_a_ and **102**_c_ adjacent to the read bit line **102**_b_ are formed at a depth or in a layer which is different from that of the read bit line **102**_b_. FIG. **3**C is a schematic view of a cross section taken along a plane including dotted line C-D in FIG. **2**A. FIG. **3**D illustrates a cross section along dotted line E-F in FIG. **3**C.

As illustrated in FIG. **3**D which is a cross-sectional view, the read bit lines **102**_a_ and **102**_c_ are formed at a depth which is different from that of the read bit line **102**_b_. In FIG. **3**D, the read bit lines are formed at two kinds of depths but may also be formed at three or more kinds of depths. Additional manufacturing steps are needed in this method; however, the parasitic capacitance between the adjacent read bit lines can be reduced compared with the method in which the read bit lines are formed in the same layer (FIG. **3**B).

For example, the height of each of the read bit lines **102**_a_ to **102**_c_ is 5 times the width thereof and the distance between the read bit lines is equal to the width thereof; when the depth of one read bit line is different from the depth of an adjacent read bit line by the height of the read bit line as illustrated in FIG. **3**D, the parasitic capacitance generated between one read bit line and another read bit line is reduced to half or less. As the height of the read bit line is increased (as the aspect ratio is increased), the effect of reducing the parasitic capacitance is improved.

When a read bit line is formed apart from a write word line, a read word line, or a capacitor as in this embodiment, most of the parasitic capacitance of the read bit line is generated between the read bit line and the other read bit lines. In particular, in order to miniaturize a wiring and reduce the resistance of the read bit line, the aspect ratio of the read bit line needs to be increased, which also increases the parasitic capacitance between the read bit lines.

Therefore, the effect of reducing the parasitic capacitance between the read bit lines by arranging the read bit lines as illustrated in FIG. **3**D is advantageous. In the case where a reduction in the parasitic capacitance between the read bit lines and a reduction in the resistance of the read bit line are expected at the same time, the read bit lines are preferably arranged as illustrated in FIG. **3**D. In this embodiment, any of the methods illustrated in FIGS. **3**B and **3**D can be employed.

In FIG. **2**A, a second insulator **103** is formed over the read bit line **102**_b_ to have an appropriate thickness. The thickness and material of each of the first insulator **101** and the second insulator **103** are important to estimate the parasitic capacitance between the read bit lines. The thickness of each of the first insulator **101** and the second insulator **103** is preferably 100 nm to 1 μm. In addition, the first insulator **101** and the second insulator **103** may each be formed using a material having a relatively low permittivity such as silicon oxide.

Next, the second insulator **103** is etched to form a contact hole, and a first contact plug **104** connected to the read bit line **102**_b_ is formed. After that, a first semiconductor film **105** is formed using polycrystalline silicon, single crystal silicon, or the like to be a film having an appropriate shape. Further, a first gate insulating film **106** is formed to cover the first semiconductor film **105**.

FIG. **4**A is a view at this stage, which is seen from the above. Here, the first gate insulating film **106** is not illustrated. In a portion where the first semiconductor film **105** is not provided, the first gate insulating film **106** is provided in contact with the second insulator **103**. In addition, the read bit lines **102**_a_ to **102**_c_ (existing below the second insulator **103**) are provided in a direction along dotted line A-B (hereinafter, also referred to as a bit line direction) in the drawing so as to overlap with the first semiconductor film **105**.

It is preferable to provide another semiconductor integrated circuit in a lower layer of the read bit lines **102**_a_ to **102**_c_ so as to increase the integration degree. This also applies to other embodiments. However, in general, in the case where the semiconductor integrated circuit is provided in the lower layer, noise caused by the circuit may hinder the operation of a transistor in an upper layer.

Against this problem, a shield layer may be provided below the transistor in the upper layer so as to absorb noise. In this embodiment, the read bit lines **102**_a_ to **102**_c_ are arranged to overlap with the first semiconductor film **105**, so that the read bit lines **102**_a_ to **102**_c_ serve as shield layers to absorb noise.

Here, a length necessary for the memory cell will be described. Portions denoted by a and d in FIG. **2**A are provided for separation between adjacent memory cells. These portions can be shared by the adjacent memory cells, and the length of each of the portions is preferably greater than or equal to 0.5F per one cell. A portion denoted by b is a portion where a gate of a read transistor is provided. The length of this portion needs to be greater than or equal to 1F for circuit formation, though the actual width of the gate can be smaller.

Further, a portion denoted by c is a portion where a write transistor is provided. In this embodiment, a channel of the write transistor is provided substantially perpendicularly to a substrate; therefore, the length of the portion denoted by c may be ideally 0, is preferably greater than or equal to 0.5F in order to improve yield, and is 1F in FIG. **2**A. From the above description, when the lengths of the portions denoted by a and d are each greater than or equal to 0.5F, the length of the memory cell needs to be greater than or equal to 2F, preferably greater than or equal to 2.5F. Note that the length of the memory cell is 3F in FIG. **2**A.

When the length of the portion denoted by d is reduced to be less than or equal to 0.5F by a known resist slimming method or the like, for example, the length of the memory cell can be 2F even if the length of the portion denoted by c is greater than 0. That is, the sum of the length of the portion denoted by d and the length of the portion denoted by c can be 0.5F.

For example, when the length of the portion denoted by d is reduced to be 0.3F by the resist slimming method, a length of 0.2F can be ensured for the portion denoted by c even if the length of the portion denoted by a and the length of the portion denoted by b are set to 0.5F and 1F, respectively. That is, the length of the memory cell is 2F. Note that in this case, a contact hole is formed in the portion denoted by d later, and thus a possibility of short circuit between wirings due to overetching is increased.

Next, a width of the memory cell will be described with reference to FIG. **4**A. Portions denoted by e and g in FIG. **4**A are provided for separation between the adjacent memory cells and each need to have a length greater than or equal to

0.5F. A portion denoted by f is a portion where the gate of the read transistor is provided and needs to have a length greater than or equal to 1F.

Particularly in the case where the gate of the read transistor is processed in a general photolithography step, the length of the portion denoted by f needs to be greater than or equal to 2F in consideration of misalignment; in the case of employing a special manufacturing method according to this embodiment, the length of the portion denoted by f can be 1F. Thus, the width of the memory cell needs to be greater than or equal to 2F. Accordingly, the area of the memory cell is $4F^2$ at a minimum, and is preferably greater than or equal to $5F^2$ in consideration of yield and the like.

<FIG **2**B>

First conductive layers **107***a* to **107***d* (note that the first conductive layers **107***c* and **107***d* are illustrated only in FIG. **4**B) serving as gates of read transistors are formed over the first gate insulating film **106**. The material and thickness of each of the first conductive layers **107***a* to **107***d* may be set as appropriate but are preferably set to be suitable for the following process. For example, polycrystalline silicon may be used.

FIG. **4**B is a view at this stage, which is seen from the above. In practice, the processing accuracy of the first conductive layers **107***a* to **107***d* is substantially equal to the processing accuracy of the first semiconductor film **105**; thus, the first conductive layers **107***a* to **107***d* might imperfectly divide the first semiconductor film **105** because of misalignment. In order to avoid such a problem, the length of each of the first conductive layers **107***a* to **107***d* in a direction perpendicular to dotted line A-B (hereinafter, also referred to as a word line direction) in FIG. **4**B may be set to 2F. In this embodiment, however, that problem can be overcome even when the length is 1F, by employing the method described below.

<FIG **2**C>

A first conductive film having an appropriate thickness is formed to cover the first conductive layers **107***a* to **107***d*. The first conductive film may be formed using a material which is the same as or different from that for the first conductive layers **107***a* to **107***d*. Then, the first conductive film is subjected to anisotropic etching, so that sidewalls **108** are formed on side surfaces of the first conductive layers **107***a* to **107***d*. The width of each of the sidewalls **108** is preferably 0.1F to 0.3F. In this manner, the above-described memory cell width of 2F can be attained.

Note that application of this technique is not limited to application to this embodiment and the gain cell. Each of the first conductive layers **107***a* to **107***d* also corresponds to a floating gate of a flash memory or the like, and application of this technique thereto contributes to miniaturization of the memory cell.

Further, the first semiconductor film **105** is doped with an impurity with the use of the first conductive layers **107***a* to **107***d* and the sidewalls **108** on the side surfaces thereof as masks, so that n-type or p-type impurity regions **109***a* to **109***d* (the impurity region **109***d* is illustrated only in FIG. **4**C) are formed. Then, a third insulator **110** is formed. A surface of the third insulator **110** is planarized so that top surfaces of the first conductive layers **107***a* to **107***d* are exposed.

FIG. **4**C is a view of the memory cell at this stage, which is seen from the above. The first conductive layers **107***a* to **107***d* and the sidewalls **108** on the side surfaces thereof are formed, and serve as the gates of the read transistors. Since the provision of the sidewalls **108** enables the gates of the read transistors to cross the first semiconductor film **105** completely, the impurity region **109***a* (or **109***c*) can be completely separated from the impurity region **109***b*/**109***d* even if some misalignment is caused in the formation of the first conductive layers **107***a* to **107***d*.

As illustrated in FIG. **4**C, conductive regions including the first conductive layers **107***a* to **107***d* and the sidewalls **108** on the side surfaces thereof each have a square shape with rounded corners when seen from the above, and the length of one side of the square is greater than 1F.

Further, the impurity regions **109***a* and **109***c* extend in the word line direction. In this embodiment, the impurity regions **109***a* and **109***c* are used as part of common wirings. Note that for an increase in conductivity, it is preferable that a silicide be formed on surfaces of the impurity regions **109***a* to **109***d* by a known salicide (self-aligned silicide) technology so that the resistance is reduced. Alternatively, a wiring having low resistance may be provided, in the word line direction, between the first semiconductor film **105** and the second insulator **103** or between the first semiconductor film **105** and the read bit lines **102***a* to **102***c*.

<FIG **6**A>

A fourth insulator, a fifth insulator, and a second conductive film are each formed to have an appropriate thickness. The fourth insulator is preferably formed using a material whose etching rate is different from that of the material for the fifth insulator formed over the fourth insulator, e.g., aluminum oxide, aluminum nitride, or silicon nitride with a thickness of 10 nm to 100 nm In the case where an oxide semiconductor is used for second semiconductor films **114***a* and **114***b* formed later, the fourth insulator is preferably formed using a material having a barrier property against hydrogen.

The thickness of the fifth insulator is determined in consideration of the height of a projecting insulator **112** formed later and the channel length of a write transistor, and is 100 nm to1 μm for example. In addition, the fifth insulator is preferably formed using a material whose etching rate is different from that of the material for the fourth insulator, and silicon oxide may be used. In addition, the material and thickness of the second conductive film may be set as appropriate and are preferably those which can provide a function of an etching stopper when a third contact plug **124** is formed later.

The second conductive film and the fifth insulator are etched, so that the projecting insulator **112** and a second conductive layer **113** thereover are formed. This etching is stopped when a surface of the fourth insulator is exposed. Since the etching rates of the fourth insulator and the fifth insulator are different from each other, the fourth insulator can be used as an etching stopper; thus, overetching of the lower layer can be prevented. After that, the fourth insulator is etched. The fourth insulator becomes a fourth insulating layer **111**.

At this stage, the projecting insulator **112**, the second conductive layer **113**, and the fourth insulating layer **111** extend substantially in the word line direction. FIG. **5**A illustrates this state seen from the above. Note that when the height of the projecting insulator **112** is denoted by Hand the distance between the projecting insulator **112** and an adjacent projecting insulator (not shown) is denoted by W, the ratio H/W is preferably greater than or equal to 1 and less than or equal to 20, further preferably greater than or equal to 5 and less than or equal to 20.

<FIG **6**B>

The island-shaped second semiconductor films **114***a* and **114***b* (note that the second semiconductor film **114***b* is illustrated only in FIG. **5**B) are formed. The second semiconductor films **114***a* and **114***b* are in contact with the first conductive layers **107***a* to **107***d*.

At this time, the second conductive layer **113** is also etched using the second semiconductor films **114***a* and **114***b* as masks. Accordingly, a portion in the second conductive layer **113** over which the second semiconductor films **114***a* and **114***b* are not provided is removed. As illustrated in FIG. **6**B, part of the second conductive layer **113** remains to become a second conductive layer **113***a*. After that, a second gate insulating film **115** is formed to cover the second semiconductor films **114***a* and **114***b*.

The thicknesses of the second semiconductor films **114***a* and **114***b* and the second gate insulating film **115** can be determined as appropriate but are preferably determined in accordance with the channel length of the transistor or the distance W between the projecting insulators, for example, may be set to 1/50 to 1/5 of the channel length or 1/10 to 1/50 of the distance W between the projecting insulators. Note that the second gate insulating film **115** may be thinned to such a level that a tunneling current or the like does not cause a problem. In addition, the second gate insulating film **115** may be formed using a material whose relative permittivity is greater than or equal to 10.

The second gate insulating film **115** may be formed using a material whose etching rate is different from that of a material used for write word lines **116***a* and **116***b* formed later or a material used for a sixth insulator **117**. In such a sense, hafnium oxide, tantalum oxide, aluminum oxide, zirconium oxide, or the like may be used. The second gate insulating film **115** may also be a multilayer film including any of the above materials. For example, a two-layer film including silicon oxide and aluminum oxide may be used. p There is no limitation on the kind of a semiconductor used for the second semiconductor films **114***a* and **114***b* but the mobility thereof is preferably higher than or equal to 5 cm$^2$/Vs. For example, polycrystalline silicon, polycrystalline germanium, polycrystalline silicon germanium, indium oxide, an oxide obtained by adding a metal element to indium oxide, gallium nitride, a compound obtained by adding oxygen to gallium nitride, gallium arsenide, indium arsenide, or zinc sulfide may be used.

In particular, in the case where the capacitance of the capacitor is reduced, the off-state resistance needs to be higher than that of a cell transistor in a 1Tr-DRAM. In order to increase the off-state resistance, for example, it is effective to significantly reduce the thickness of each of the second semiconductor films **114***a* and **114***b* to 0.5 nm to 5 nm Further, it is also preferable to increase the height of the projecting insulator (or the channel length of the write transistor). Alternately, when the original mobility is higher than or equal to 200 cm$^2$/Vs as in the case of polycrystalline silicon, the mobility may be reduced to approximately 10 cm$^2$/Vs by increasing the nitrogen concentration or the carbon concentration of the semiconductor region to $1\times10^{19}$ cm$^{-3}$ to $5\times10^{20}$ cm$^{-3}$.

It is preferable to further increase the off-state resistance of the write transistor because the refresh interval of the memory cell can be lengthened. For example, when the off-state resistance is million times or more that of a general cell transistor in a 1Tr-DRAM, the memory cell can be used practically without refresh operation.

In order to obtain such a very high off-state resistance, silicon (whose band gap is 1.1 eV) is inadequate. It is necessary to use a wide band gap semiconductor whose band gap is greater than or equal to 2.5 eV and less than or equal to 4 eV, preferably greater than or equal to 3 eV and less than or equal to 3.8 eV. For example, an oxide semiconductor such as indium oxide or zinc oxide, a nitride semiconductor such as gallium nitride, or a sulfide semiconductor such as zinc sulfide may be used.

The off-state resistance is inversely proportional to the concentration of carriers excited by heat. Since the band gap of silicon is 1.1 eV even when carriers caused by donors or acceptors do not exist at all (intrinsic semiconductor), the concentration of carriers excited by heat at room temperature (300 K) is approximately $1\times10^{11}$ cm$^{-3}$.

On the other hand, in the case of a semiconductor whose band gap is 3.2 eV, the concentration of carriers excited by heat is approximately $1\times10^{-7}$ cm$^{-3}$. When the electron mobility is the same, the resistivity is inversely proportional to the carrier concentration, so that the resistivity of the semiconductor whose band gap is 3.2 eV is 18 orders of magnitude higher than that of silicon.

It is preferable that the concentration of carriers caused by donors or acceptors be as low as possible, e.g., lower than or equal to $1\times10^{12}$ cm$^{-3}$. The threshold voltage of the transistor depends on the concentration of carriers caused by donors or acceptors. Patent Document 3 can be referred to for such a wide band gap semiconductor.

<FIG **6**C>

A third conductive film is formed and subjected to anisotropic etching to form the write word lines **116***a* and **116***b*. The width of each of the write word lines **116***a* and **116***b* substantially equals to the thickness of the third conductive film. Patent Document 4 may be referred to for a technique for forming a wiring at a side surface of the projecting insulator in a self-aligned manner as described above. Further, the sixth insulator **117** which has a flat surface is formed.

In the case where a top of the write word line **116***a* and a top of the write word line **116***b* are positioned at a higher level than a top of the projecting insulator **112** (or at substantially the same level as the second conductive layer **113***a*), the write word lines **116***a* and **116***b* might be in contact with the third contact plug **124** which is formed later. Therefore, the height of each of the write word lines **116***a* and **116***b* is preferably greater than or equal to 30% and less than or equal to 90%, further preferably greater than or equal to 40% and less than or equal to 80% of the height of the projecting insulator **112**.

Through the above, the second conductive layer **113***a* and the write word lines **116***a* and **116***b* may be in an offset state (a state where the second conductive layer **113***a* and the write word lines **116***a* and **116***b* do not overlap with each other). In order to prevent a short-channel effect, it is preferable to provide an offset region (a portion where the second conductive layer **113***a* and the write word lines **116***a* and **116***b* do not overlap with each other) which is 10 nm to 50 nm long in the perpendicular direction or has a length that is 20% to 100% of the height of each of the write word lines **116***a* and **116***b*.

Note that the drawing illustrates the case where the write word lines **116***a* and **116***b* and the first conductive layers **107***a* to **107***d* are in an offset state; in the case where the integration degree is increased so that the length of the portion denoted by c in FIG. **2**A becomes 0, the write word lines **116***a* and **116***b* overlap with the first conductive layers **107***a* to **107***d* inevitably.

Such a state might lead to an unnecessary change in potential in charging of the capacitor. However, in the case where the aspect ratio of each of the write word lines **116***a* and **116***b* is greater than or equal to 5 and less than or equal to 20, the parasitic capacitance generated between the write word lines **116***a* and **116***b* and the first conductive layers **107***a* to **107***d* is approximately 20% of gate capacitance (capacitance caused by overlapping of the write word lines **116***a* and **116***b* with the second semiconductor films **114***a* and **114***b*) at most, which is ignorable when the capacitance of the capacitor is set to be twice or more of the gate capacitance.

Further, an impurity may be implanted into the second semiconductor films **114***a* and **114***b* with the use of the write word lines **116***a* and **116***b* as masks by an ion implantation method or the like to form an n-type or p-type region (doped region). In the case where the distances from portions where the first conductive layers **107***a* to **107***d* are in contact with the second semiconductor films **114***a* and **114***b* to the write word lines **116***a* and **116***b* are each less than or equal to 30 nm, preferably less than or equal to 10 nm, the doped region is not necessarily formed.

Further, the doped region is not necessarily formed either, in the case where the second semiconductor films **114***a* and **114***b* have any conductivity type from the beginning and the transistor can be controlled by utilizing a difference in work function between the semiconductor material for the second semiconductor films **114***a* and **114***b* and the material for the write word lines **116***a* and **116***b*. For example, polycrystalline silicon over silicon oxide has n-type conductivity even when it is not doped with impurities; electrons are removed by using a material having a work function higher than or equal to 5 eV such as indium nitride, zinc nitride, or p-type silicon for the write word lines **116***a* and **116***b*, so that an n-channel transistor whose threshold voltage is higher than or equal to +1 V can be formed.

<FIG **7**A>

The sixth insulator **117** is etched so that contact holes are formed, and second contact plugs **118***a* to **118***d* (note that the second contact plugs **118***c* and **118***d* are illustrated only in FIG. **5**B) are embedded therein.

FIG. **5**B is a view at this stage, which is seen from the above. Note that the second gate insulating film **115** is not illustrated in FIG. **5**B. The second conductive layer **113***a* exists under a portion which is in the second semiconductor film **114***a* and interposed between the write word line **116***a* and the write word line **116***b*. Further, in a portion which is interposed between the write word line **116***a* and the write word line **116***b* and covered with none of the second semiconductor films **114***a* and **114***b*, the projecting insulator **112** is exposed. That is, the second conductive layer **113***a* is isolated.

<FIG **7**B>

A seventh insulator **119** is formed using a material having a relatively low permittivity such as silicon oxide or silicon oxycarbide. Holes are formed in the seventh insulator **119** to form capacitors therein. Then, capacitor electrodes **120***a* and **120***b* each having a thickness of 2 nm to 20 nm are formed on inner walls of the holes. The maximum thickness of each of the capacitor electrodes **120***a* and **120***b* may be determined in accordance with the feature size F. The thickness is preferably less than or equal to 5 nm when F is 20 nm, and the thickness is preferably less than or equal to 2.5 nm when F is 10 nm

Further, a capacitor insulator **121** having a thickness of 2 nm to 20 nm is formed. The capacitor insulator **121** can be formed using any of various high-k materials, preferably hafnium oxide, zirconium oxide, tantalum oxide, barium strontium titanate, or the like.

<FIG **7**C>

Read word lines **122***a* and **122***b* are formed in the word line direction. The capacitor electrode **120***a* (or **120***b*), the capacitor insulator **121**, and the read word line **122***a* (or **122***b*) form a capacitor.

Further, an eighth insulator **123** is formed, and the third contact plug **124** is embedded therein. The seventh insulator **119** and the eighth insulator **123** are sufficiently thick; thus, when misalignment of a mask and excessive etching occur at the same time, a contact hole could be connected to the write word line **116***a* or **116***b*. Such a problem is likely to be caused in the case where the integration degree is high and the width of the top of the projecting insulator **112** is processed at a feature size.

In order to avoid such a problem, it is preferable that the second conductive layer **113***a* be sufficiently thick and the tops of the write word lines **116***a* and **116***b* be positioned at a sufficiently lower level than a top of the second conductive layer **113***a*. In that case, the second conductive layer **113***a* is preferably formed using a material which functions as an etching stopper.

Then, write bit lines **125***a* and **125***b* (note that the write bit line **125***b* is illustrated only in FIG. **5**C) are formed in the bit line direction. In this manner, gain memory cells each including two transistors and one capacitor can be manufactured. FIG. **5**C is a view at this stage, which is seen from the above. Note that the eighth insulator **123** is not illustrated in FIG. **5**C. A circuit diagram of this embodiment corresponds to FIG. **1**.

(Embodiment 2)

This embodiment will be described with reference to FIG. **8**. In this embodiment, a circuit (a driver circuit **202**) for driving a memory cell, such as a sense amplifier or a decoder, is formed on a surface of a substrate **201** of a single crystal semiconductor by known techniques for forming a semiconductor integrated circuit. A read bit line **203** is formed over the driver circuit **202**, and a memory cell layer **204** including a write word line and a read word line is provided over the read bit line **203**. Further, a write bit line **205** is formed over the memory cell layer **204**.

(Embodiment 3)

A manufacturing process of a memory cell according this embodiment will be described with reference to FIGS. **9**A to **9**C and FIGS. **10**A to **10**C. FIGS. **9**A to **9**C and FIGS. **10**A to **10**C are cross-sectional views illustrating the manufacturing process of the memory cell according to this embodiment. In this embodiment, with a few exceptions, just the outline is described. Embodiment 1, known techniques for forming a semiconductor integrated circuit, or the like may be referred to for the details. FIGS. **9**A to **9**C and FIGS. **10**A to **10**C will be described below in this order.

<FIG **9**A>

A read bit line **302** is formed over a first insulator **301**. Further, a second insulator **303** is formed over the read bit line **302** to have an appropriate thickness. The thickness of each of the first insulator **301** and the second insulator **303** is preferably 100 nm to 1 μm. In addition, the first insulator **301** and the second insulator **303** may each be formed using a material having a relatively low permittivity such as silicon oxide.

Next, the second insulator **303** is etched to form a contact hole, and a first contact plug **304** connected to the read bit line **302** is formed. After that, a first semiconductor film **305** is formed using polycrystalline silicon, single crystal silicon, or the like to be a film having an appropriate shape. Further, a first gate insulating film **306** is formed to cover the first semiconductor film **305**.

First conductive layers **307***a* and **307***b* serving as gates of read transistors are formed over the first gate insulating film **306**. As in Embodiment 1, sidewalls may be provided on side surfaces of the first conductive layers **307***a* and **307***b* with the use of a conductive material. Further, an impurity region may be provided in the first semiconductor film **305** with the use of the first conductive layers **307***a* and **307***b* as masks. Then, a third insulator **308** is formed. A surface of the third insulator **308** is planarized so that top surfaces of the first conductive layers **307***a* and **307***b* are exposed.

<FIG 9B>

The third insulator **308** is partly etched to form a third insulator **308***a*. At this time, a portion interposed between the first conductive layers **307***a* and **307***b* is left. Further, a fourth insulator, a fifth insulator, and a second conductive film are each formed to have an appropriate thickness. For the fourth insulator, the fifth insulator, and the second conductive film, the fourth insulator, the fifth insulator, and the second conductive film in Embodiment 1 may be referred to.

Through etching, a fourth insulating layer **309** is processed from the fourth insulator, and a projecting insulator **310** and a second conductive layer **311** are formed. As in Embodiment 1, at this stage, the projecting insulator **310**, the second conductive layer **311**, and the fourth insulating layer **309** extend substantially in the word line direction.

<FIG 9C>

An island-shaped second semiconductor film **312** is formed. The second semiconductor film **312** is in contact with the first conductive layers **307***a* and **307***b*. At this time, the second conductive layer **311** is also etched using the second semiconductor film **312** as a mask. Accordingly, a portion in the second conductive layer **311** over which the second semiconductor film **312** is not provided is removed.

After that, a second gate insulating film **313** is formed to cover the second semiconductor film **312**, the first conductive layers **307***a* and **307***b*, and the first gate insulating film **306**.

For the second semiconductor film **312** and the second gate insulating film **313**, the second semiconductor films **114***a* and **114***b* and the second gate insulating film **115** in Embodiment 1 may be referred to, respectively.

<FIG 10A>

A third conductive film **314** is formed to cover the second gate insulating film **313**.

<FIG 10B>

The third conductive film **314** is subjected to anisotropic etching, so that third conductive layers **314***a* to **314***d* are formed. The third conductive layers **314***a* to **314***d* are formed in the word line direction along the projecting insulator **310**, the first conductive layers **307***a* and **307***b*, and the third insulator **308***a*.

Thus, the third conductive layers **314***a* and **314***b* serve as write word lines. The third conductive layers **314***c* and **314***d* form capacitors with the first conductive layers **307***a* and **307***b*, respectively, with the second gate insulating film **313** used as a dielectric (capacitor insulator), and serve as read word lines.

<FIG 10C>

A sixth insulator **315** is formed and etched so that a contact hole reaching the second conductive layer **311** is formed, and a second contact plug **316** is embedded therein. Further, a write bit line **317** is formed in the bit line direction. In this manner, gain memory cells each including two transistors and one capacitor can be manufactured. The area of the memory cell according to this embodiment can also be $4F^2$ at a minimum.

The memory cell according to this embodiment has a simple structure and is manufactured by fewer steps as compared with the memory cell in Embodiment 1. Moreover, the first conductive layer **307***a* and the third conductive layer **314***cc*(or the first conductive layer **307***b* and the third conductive layer **314***d*) form the capacitor of the memory cell. The capacitance of the capacitor is determined in accordance with the height of the first conductive layer **307***a* (or the first conductive layer **307***b*).

(Embodiment 4)

A manufacturing process of a memory cell according this embodiment will be described with reference to FIGS. **11**A to **11**C and FIGS. **12**A and **12**B. FIGS. **11**A to **11**C and FIGS. **12**A and **12**B are cross-sectional views illustrating the manufacturing process of the memory cell according to this embodiment, along line G-H and line I-J. Line G-H and line I-J cross each other perpendicularly at the point X. Line G-H is parallel to bit lines and line I-J is parallel to word lines. Thus, the direction of line G-H and the direction of line I-J are also called the bit line direction and the word line direction, respectively.

In this embodiment, with a few exceptions, just the outline is described. The above embodiments, known techniques for forming a semiconductor integrated circuit, or the like may be referred to for the details. FIGS. **11**A to **11**C and FIGS. **12**A and **12**B will be described below in this order.

<FIG **11**A>

Device isolation insulators **402** are formed in a semiconductor substrate **401**. Single crystal silicon may be used for the semiconductor substrate **401**. Further, a first gate insulating film **403** and a first conductive layer **404** are formed. The first conductive layer **404** is a memory node of the memory cell, and formed so as cross a region between two device isolation insulators **402**. Further, impurity regions **405** are formed by a self-aligned method using the first conductive layer **404** as a mask.

A transistor is formed where the first conductive layer **404** is the gate and the first gate insulating film **403** is the gate insulating film. This transistor functions as a read transistor. Further, the impurity regions **405** are extended in the bit line direction and at least one of them functions as a read bit line.

Further, a first insulator **406** is provided so as to cover the upper surface, the side face toward I and the side face toward J of the first conductive layer **404**. Second conductive layers **408** are formed at the side faces toward G and H where a second insulator **407** is interposed therebetween. The first conductive layer **404** and the second conductive layers **408** form capacitors, where the second insulator **407** is a dielectric. The second conductive layers **408** are formed by an anisotropic etching method as shown in Embodiment 3. Note that the second conductive layers **408** function as read word lines.

The first conductive layer **404** may be formed as follows. First, a conductive film for forming the first conductive layer **404** is formed over the first gate insulating film **403**, and is patterned in line shape that is long in the bit line direction. Then the impurity regions **405** are formed by implantation of impurity ions.

Next, an insulating film which is for forming the first insulator **406** is formed and its surface is flattened. The insulating film is selectively etched to the surface of the semiconductor substrate **401** and is patterned in line shape long along the word line direction. As a result, the first conductive layer **404** is rectangular (or square) when seen from the above.

Then, the second insulator **407** is formed. Further, a conductive film which is for forming the second conductive layers **408** is formed and is anisotropically etched, so the second conductive layers **408** are formed on the side faces of the first conductive layer **404** (and the side faces of the first insulator **406**). As a result, the second conductive layers **408** are extended in the word line direction.

<FIG **11**B>

Third insulators **409** are formed by depositing an insulator and flattening its surface. FIG. **11**B shows that a part of the second insulator **407** is etched off by the flattening process. However, the second insulator **407** may remain.

<FIG. **11**C>

A third conductive layer **410** extending toward the word line direction is formed. Further, a fourth insulator **411** is formed over the third conductive layer **410**. The surface of the fourth insulator **411** is flattened. Then, an opening portion **412** to the first conductive layer **404** is formed.

<FIG **12**A>

The opening portion **412** is filled by forming a second gate insulating film **413** on the side face of the opening portion **412**, and forming a pillar semiconductor **414**. Accordingly, a transistor is formed where the third conductive layer **410** and the second gate insulating film **413** are the gate and the gate insulating film, respectively. The third conductive layer **410** functions as a write word line. Note that the diameter of the opening portion **412** is determined in accordance with the channel width of the transistor and may be 10 nm to 50 nm, for example. Further, the thickness of the third conductive layer is determined in accordance with the channel length of the transistor and may be 100 nm to 500 nm, for example.

<FIG **12**B>

A fourth conductive layer **415** in contact with the pillar semiconductor **414** is formed. The material used for the fourth conductive layer **415** may be determined in accordance with the semiconductor material of the pillar semiconductor **414**. Further, a fifth insulator **416** is formed, and a contact plug **417** to the fourth conductive layer **415** is embedded. Then, a fifth conductive layer **418** extending toward the bit line direction is formed. The fifth conductive layer **418** functions as a write bit line.

In this manner, a gain memory cell including two transistors and two capacitors can be manufactured. The area of the memory cell according to this embodiment can be $4F^2$ at a minimum. The first conductive layer **404** and the second conductive layers **408** form the capacitors of the memory cell. The capacitance of each of the capacitors can be determined in accordance with the height of the first conductive layer **404**.

This application is based on Japanese Patent Application serial no. 2011-031788 filed with the Japan Patent Office on Feb. 17, 2011, the entire contents of which are hereby incorporated by reference.

What is claimed is:

**1**. A semiconductor device comprising:

a substrate

a read bit line in or over the substrate;

a conductor over the read bit line;

a read word line over the read bit line, the read word line being designed to be parallel to the write word line;

a write word line over the conductor;

a semiconductor facing the write word line with a gate insulating film therebetween; and

a write bit line over the semiconductor and the read bit line, the write bit line being designed to be parallel to the read bit line,

wherein the write word line is configured to control a conductivity of the semiconductor so that the write bit line and the conductor are electrically connectable via the semiconductor by a potential of the write word line to store charges in the conductor in accordance with a potential of the write bit line, and

wherein the read word line is designed to form a capacitor with the conductor.

**2**. The semiconductor device according to claim **1**, further comprising a semiconductor region,

wherein the conductor is configured to control a conductivity of the semiconductor region by a potential of the conductor.

**3**. The semiconductor device according to claim **1**, wherein the read word line is on a side face of the conductor with an insulating film therebetween.

**4**. The semiconductor device according to claim **3**, wherein the write word line is over the conductor with the insulating film therebetween.

**5**. The semiconductor device according to claim **1**, further comprising a circuit,

wherein the read bit line is over the circuit, and

wherein the read bit line is designed to work as a shielding layer for blocking a noise between a layer over the read bit line and the circuit.

**6**. A semiconductor device comprising:

a substrate;

a read bit line in or over the substrate;

a conductor over the read bit line;

a read word line over the read bit line, the read word line being designed to be parallel to the write word line;

a write word line over the conductor;

a semiconductor facing the write word line with a gate insulating film therebetween; and

a write bit line over the semiconductor and the read bit line, the write bit line being designed to be parallel to the read bit line,

wherein the write word line is configured to control a conductivity of the semiconductor so that the write bit line and the conductor are electrically connectable via the semiconductor by a potential of the write word line to store charges in the conductor in accordance with a potential of the write bit line,

wherein the read word line is designed to form a capacitor with the conductor,

wherein a portion of the semiconductor is designed to work as a channel of a write transistor of a gain cell,

wherein a portion of the write word line is designed to work as a gate of the write transistor of the gain cell, and

wherein a portion of the conductor is designed to work as a gate electrode of a read transistor of the gain cell.

**7**. The semiconductor device according to claim **6**, further comprising a semiconductor region,

wherein the conductor is configured to control a conductivity of the semiconductor region by a potential of the conductor.

**8**. The semiconductor device according to claim **6**, wherein the read word line is on a side face of the conductor with an insulating film therebetween.

**9**. The semiconductor device according to claim **8**, wherein the write word line is over the conductor with the insulating film therebetween.

**10**. The semiconductor device according to claim **6**, further comprising a circuit,

wherein the read bit line is over the circuit, and

wherein the read bit line is designed to work as a shielding layer for blocking a noise between a layer over the read bit line and the circuit.

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